Notice of Allowability	Application No.	Applicant(s)	
	10/822,167	CHAE ET AL.	
	Examiner	Art Unit	
	Eric Wendler	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Request for Continued Examination filed on July 5, 2006*.

2. ☒ The allowed claim(s) is/are *1-21*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *updated EAST search history*.

7/23/06

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

DETAILED ACTION

1. This office action is responsive to the following communications: the Request for Continued Examination filed on July 5, 2006.

2. Claims 1-21 are pending in the present application. Claims 1, 7, 13, 19, are independent claims.

Priority

3. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. KR 2003-21969, filed on April 8, 2003, and parent Application No. KR 2003-79510, filed on November 11, 2003.

Allowable Subject Matter

4. Claims 1-21 are allowed.

5. The following is an examiner's statement of reasons for allowance: regarding independent claims 1, 7, 13, the prior art of record teaches multi-chip memory systems, some which have separate sector addresses for each chip, and some which have sector addresses arranged continuously across the whole memory system, address clock drivers that generate clock signals having a chip select or enable signal and an address count-up signal, address counters that generate chip and sector information, control circuits that generate the address count-up signal, and the other peripheral claimed circuitry (buses, register, etc.). While all the elements are present in the prior art, and exist in various partial manifestations as listed below in the conclusions concerning pertinent prior art, the prior art of record fails to teach all these claimed

elements as a part of a single system. Furthermore, adequate motivation to combine large numbers of relevant references together is lacking for the elements as claimed by the applicant. Therefore, independent claims 1, 7, 13, are deemed allowable. Regarding independent claim 19, it encompasses the same subject matter as claims 1, 7, 13, expect it drafts the invention in method format rather than apparatus format. Claim 19 is therefore deemed allowable for the same reasons claims 1, 7, 13, are deemed allowable. Claims 2-6, 8-12, 14-18, 20-21, are dependent upon the allowable independent claims 1, 7, 13, 19, and are therefore also deemed allowable.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

6. Applicant's arguments, see Remarks, pages 6-8, filed July 5, 2006, with respect to claims 1-21 have been fully considered and are persuasive. The rejections of claims 1-21 have been withdrawn.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Oguchi et al. (5,332,922) teach a multi-chip memory system with clock drivers and counters, but fails to teach a clock driver with chip enable and count-up inputs. Roohparvar (6,278,654) teaches a synchronous flash memory system in which the memory system receives a chip enable signal and a clock signal, but sector

addressing is not taught as being across the whole memory system. Shiga et al. (US 2003/0117886) teach a memory device with multiple blocks that has can separately erase each block. Choi et al. (5,625,590) teach a memory system with an address driver and clock generator that generates a clock signal to a memory array with a count-up signal as an input, but there are not multiple chips or a chip select signal. Sakui et al. (6,097,666) teach address clock drivers and counters with an address count-up signal as the input, but the structure is different and there are not multiple chips with sector addresses across the memory system. Fukuzumi (5,910,917) teaches a command control unit with a chip enable signal, and a serial clock generator to generate a clock signal for multiple chips, but the structure is different and there are not multiple chips with sector addresses across the memory system. Sugio (US 2006/0077721) teaches multi-chip memory system with an address driver, chip enable signal, and a clocking signal, but the address driver does not have a count-up signal input, and the sector addresses are not across the memory system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Wendler whose telephone number is (571) 272-5063. The examiner can normally be reached on Monday - Friday 9:00 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EJW
7/20/06